

WE ARE HIRING: Senior DFT Engineer

Location: Ho Chi Minh, Vietnam

Employment Type: Full-time

About Faraday

Faraday Technology Corporation is a leading **fabless ASIC and IP provider** with over **30 years of global semiconductor experience**. Headquartered in Taiwan, Faraday delivers thousands of successful SoC and ASIC designs annually and supports customers worldwide across automotive, AI, networking, consumer electronics, and IoT

Job Overview

We are seeking a highly motivated **Senior DFT Engineer** to join our advanced ASIC design team. In this role, you will lead the definition and implementation of comprehensive Design-for-Test (DFT) strategies for complex SoCs and IPs. You will work closely with Front-end, Backend, and Product Engineering teams to ensure high test coverage, optimal yield, and cost-effective manufacturing solutions.

Key Responsibilities

- **DFT Strategy & Architecture:** Define DFT specifications and finalize comprehensive strategies (MBIST, SCAN, BSCAN, IP-Test, In-system test, and Low-Power DFT) to meet rigorous testing targets and quality goals.
- **Implementation & Verification:** Lead the implementation and verification of DFT circuits, ensuring robustness across various design scenarios.
- **Timing Closure:** Define DFT-specific SDC (Synopsys Design Constraints), and collaborate closely with Backend Engineers to validate timing constraints and achieve timing closure in test modes.
- **Pattern Generation & Silicon Debug:** Generate tester patterns using industry-standard tools; perform silicon bring-up, debug analysis, and failure diagnosis to resolve yield issues.
- **Optimization:** Analyze test coverage metrics and drive initiatives to improve coverage while reducing test costs, pin counts, and test time.
- **Project Leadership:** Serve as a Project Leader or Block Coordinator to manage project schedules, mitigate risks, and ensure on-time tape-out (T/O).

Qualifications & Skills

- **Education:** BS or MS degree in Electrical Engineering (EE), Computer Science (CS), or related fields.
- **Experience:** Minimum 2 years of hands-on experience in DFT implementation for ASIC/SoC designs.
 - *Note: Candidates with 8+ years of experience will be considered for Senior Manager or Technical Lead positions.*
 - *Note: Candidates with less than 2 years of experience may be considered for Junior Engineer positions*
- **Tool Proficiency:** Expert knowledge of industry-standard EDA tools, especially **Siemens EDA Tessent** (Shell, MBIST, Compression), **Synopsys TetraMAX/TestMax**, and flows involving Synthesis, Simulation, and Formal Verification.
- **Scripting & Automation:** Strong expertise in scripting languages (**Tcl, Perl, Csh**). *Familiarity with AI prompting techniques to enhance engineering productivity is a plus.*
- **Soft Skills:** Excellent communication skills (written and verbal) and proven teamwork spirit.
- **Language:** Fluent in English is required for effective customer interaction and global collaboration.

Why Join Faraday?

- Work on cutting-edge Advanced FinFET technologies with global top-tier clients.
- Be part of a truly global team with opportunities to collaborate across Asia and the US.
- Competitive compensation package and career growth opportunities in a leading ASIC design service company.
- Collaborative culture that values innovation and technical excellence.

How to Apply

- Send your **CV** to: fvttalent@faraday-tech.com
- Or apply via: **Faraday Careers Page** - <https://www.linkedin.com/jobs/view/4415187872/>