WE ARE HIRING: RTL Design Engineer
Location: Ho Chi Minh, Vietnam
Employment Type: Full-time

Job Overview

We are seeking experienced and motivated **RTL Design Engineers** to join our growing team at Faraday Technology. As a world-leading ASIC design service company, we offer opportunities to work on cutting-edge SoC projects involving high-speed interfaces and advanced process nodes. Successful candidates will be responsible for the full front-end design flow, from micro-architecture definition to netlist delivery and verification.

*Note: Candidates with 8+ years of experience will be considered for **Technical Lead** positions, while those with less experience will be hired as **Junior/Mid-level Engineers**.*

Key Responsibilities

- **Micro-architecture & RTL Coding:** Define micro-architecture specifications and develop high-quality, synthesizable RTL code using **Verilog** and **SystemVerilog**.
- **Verification & Simulation:** Perform subsystem simulation to ensure functional correctness before handoff.
- **RTL Quality Assurance:** Execute and pass comprehensive RTL QA checks, including:
    - Clock Domain Crossing (**CDC**) analysis
    - Lint checking (coding style and synthesis rules)
    - SDC (Synopsys Design Constraints) validation
- **Logic Synthesis:** Perform RTL-to-Netlist synthesis using industry-standard tools and optimize for PPA (Power, Performance, Area).
- **Post-Synthesis QA:** Ensure netlist quality by passing:
    - Logic Equivalence Checking (**LEC**)
    - Static Timing Analysis (**STA**)
    - In-house Design Kit (IDK) rule checks
- **Model Generation:** Generate Hierarchical Data Model (**HDM**) / CDC abstraction models for SoC-level integration.

- **Documentation:** Create and maintain detailed subsystem design documents and deliver complete database packages.

Qualifications & Requirements

- **Education:** BS or MS degree in Electrical Engineering (EE), Computer Science (CS), or related fields.
- **Experience:** Minimum **2 years** of working experience in RTL design.
    - Strong preference for candidates with experience in **high-speed interface designs** (e.g., **PCIe**, **Ethernet**, USB, DDR).
- **Technical Skills:**
    - Proficient in **SystemVerilog** and Verilog HDL.
    - Solid understanding of digital logic design principles and synchronous circuit design.
    - Familiarity with standard bus protocols: **AMBA AXI, AHB, APB**.
    - Knowledge of **PCIe Gen-4/Gen-5** specifications is highly desirable.
- **EDA Tool Proficiency:** Hands-on experience with front-end EDA tools:
    - **Simulation:** Cadence Xcelium or Synopsys VCS
    - **Synthesis:** Synopsys Design Compiler (DC)
    - **Static Timing Analysis:** Synopsys PrimeTime (PT)
    - **Linting:** Synopsys VC SpyGlass Lint or similar
    - **Formal Verification (LEC):** Cadence Conformal or Synopsys Formality
    - **CDC Analysis:** Synopsys SpyGlass CDC or Mentor Graphics Questa CDC
- **Language:** Good English communication skills (written and verbal) for technical documentation and global team collaboration.

Preferred Qualifications (For Senior/Lead Roles)

- 8+ years of relevant experience in ASIC/SoC design.
- Proven track record of leading subsystem design projects from specification to tape-out.
- Experience mentoring junior engineers and conducting code/design reviews.

- Deep expertise in low-power design methodologies (UPF) is a plus.

Why Join Faraday Technology?

- Work on diverse projects across various industries (AI, Automotive, High-Performance Computing, Mobile).
- Access to the latest advanced process nodes (5nm, 3nm, and beyond).
- Collaborative environment with opportunities for continuous learning and career growth.
- Competitive compensation package and benefits.

How to Apply

- Send your **CV** to: ftvtalent@faraday-tech.com
- Or apply via: **Faraday Careers Page -** https://www.linkedin.com/jobs/view/4424496704/